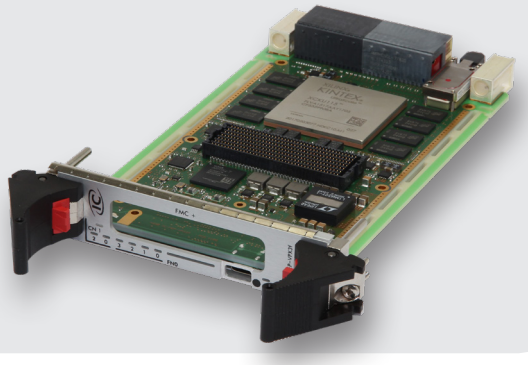
IC-FEP-VPX3f

3U VPX VITA 66.5 FPGA board with FMC+ Site

- *3U VPX - VITA 66.5*
- *1*Kintex® UltraScale™ FPGA*
- *2* DDR4 banks (up to 4GB each)*
- *1*Artix-7 control node*
- *1*FMC+ site (VITA 57.4)*



Based on the latest Xilinx 20nm FPGA family, the **IC-FEP-VPX3f** enhances the front-end processing (FEP) product line of Interface Concept, as the first VITA 66.5 compliant FPGA board on the market today.

The Kintex® UltraScale™ FPGA provides a better performance/power consumption ratio compared to previous FPGAs, and makes the **IC-FEP-VPX3f** the perfect solution for applications requiring DSP intensive processing in a 3U VPX form factor.

The **IC-FEP-VPX3f** and other IC building blocks (Intel® and PowerPC SBCs, Ethernet Switches & Routers, FMC) running our Signal Processing Reference Design are the ideal platforms to users who are willing to streamline development by concentrating their efforts on their most strategical tasks.

Description

The **IC-FEP-VPX3f** takes advantage of Kintex® UltraScale™ family capabilities and features by offering scalability, performance, connectivity and reliability in a range of environments

The Kintex® UltraScale™ FPGA built on a high performance, low power 20nm process technology is available in multiple models providing different features while keeping the same packageand footprint. Hence, the **IC-FEP-VPX3f** is available with a selection of 3 FPGAs (KU060, KU085 or KU115), and speed grades 1, 2 & 3.

The FPGA 2133MB/s bus interfaces with the 2 DDR4 banks remove bottleneck in DSP and packet processing, maximizing the board transfer performance. The Fabric Links of the VPX backplane are connected to the FPGA GTHs (FPGA dependent) transceivers, allowing data rates up to 16.3 Gbps, and 28 GPIO's.

The Embedded Hard IP Resources can be used to implement PCI Express Gen2/Gen3 (FPGA dependent) links, as well as the 10 Gigabit Ethernet ports (XAUI, 10GBase-KR) or Xilinx Aurora.

The FMC+ site of the **IC-FEP-VPX3f** is compliant with the FPGA Mezzanine Card standard (VITA 57.4), supporting plug in FMC modules provided by IC or developed by users.

The **IC-FEP-VPX3f** benefits from the latest enhancements in Kintex® UltraScale™ regarding power reduction and is available in standard, air-cooled to conduction-cooled grades (85°C).

Furthermore, Kintex® UltraScale™ interfaces with a local flash for local storage of up to 2 bitstreams. It supports secured bitstreams and partial reconfiguration.

Due to the modularity of the FPGA, the **IC-FEP-VPX3f** is compliant with several Module Profiles of the OpenVPX standard (TBD).

The **IC-FEP-VPX3f** is compliant with 3U module definitions of the VITA 46.0 standard, and optionally with the VITA 66.5 standard when it is populated with the LightConex™ transceivers.

It is available in air-cooled and conduction cooled versions compliant with VITA 47 classes

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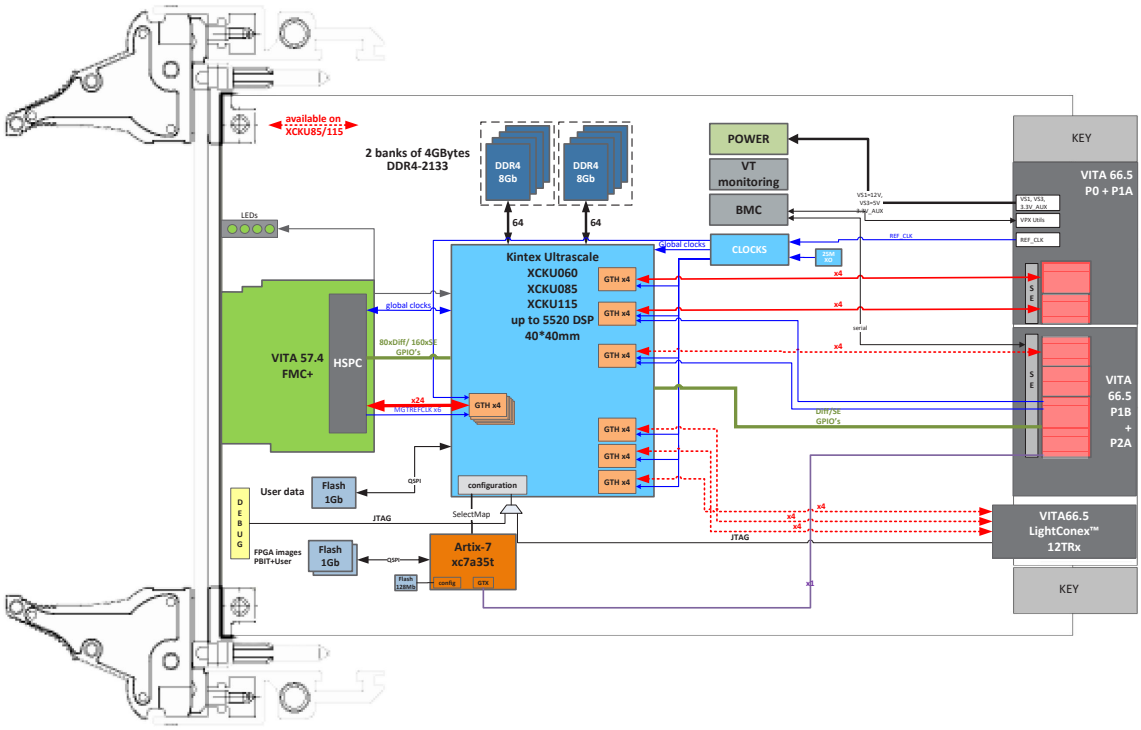
Block Diagram



Main features

Processing Unit

- Kintex® UltraScale™ KU060, KU85 or KU115
- Two banks of DDR4: 64-bit wide, up to 4GB each
- 2 * 128 MBytes of QSPI flash (bitstreams storage)
- 1 * 128 MBytes of QSPI flash (User Data storage)

VPX Interfaces

- Up to three 4-lane fabric ports on P1/P2
  - 3 * GTH x4 (Fat Pipes P1A, P1B) (*)
  - Optional 3 * GTH x4 to LightConex™ 12TRX (*)

  (*) depending on FPGA models
- 28 GPIO's from FPGA on P2, usable as single-ended or differential pairs

FMC+ VITA 57.4 interfaces

- 6 * GTH x4 links
- 80 differential pairs
- 6 reference clocks

Miscellaneous

- PIC µ-controller for System Management to VITA 46.11
- 4 LEDs

Accessories

- Engineering kit : JTAG ports for direct FPGA configuration
- Rear Transition Module

Interface features

P0 connector

- VS3, 3V3_AUX, VS1 (+12V for FMC)
- REF_CLK
- I2C bus, utilities (SYSRESET, NVMRO, GAx)

P0 + P1A connector

- Two 4-lane fabric ports
- PIC RS232

P1B + P2A connector

- One 4-lane fabric port
- 28 GPIO's

P2B connector (VITA 66.5)

- LightCONEX™ LC 150G optical engine
- 12Tx + 12Rx @ 12.5 Gbps/lane
- 24 fibers Multimode interface

FMC connector

- 24 * GTH (*)
- 80 or 160 differential pairs
- 6 clocks (LVDS Diff)

On-board firmware

The **IC-FEP-VPX3f** hardware platform is compatible with Xilinx development tools Vivado TM , Platform cable, etc.

Interface Concept provides

- VHDL code for system services (DDR4, PCIe, Aurora, IC FMC interfaces, etc.) and reference designs such as PCIe DMA Engine, signal capture & processing, etc.
- Host drivers for our CPU (Linux, VxWorks)

Customers can implement their own real-time applications with the capability to integrate existing Open Source code or third-party IP cores.

Grades

Criterion	Coating	Operation Temperature	Rec. Airflow	Oper. HR% no cond.	Storage Temperature	Sinusoidal Vibration	Random Vibration	Shock 1/2 Sin. 11ms
Standard	Optional	0 to 55°C	1 .. 2 m/s	5 to 90%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Extended	Yes	-20 to 65°C	2 .. 3 m/s	5 to 95%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Rugged	Yes	-40 to 75°C or 85° C (*)	2 .. 5 m/s	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 71°C	Yes	-40 to 71°C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 85°C	Yes	-40 to 85° C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.1g2 /Hz [10..2000]Hz	40G

(*) : Temperature grades are subject to availability according to IC products. Please consult us.

All information contained herein is subject to change without notice.

For more information, please contact:

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