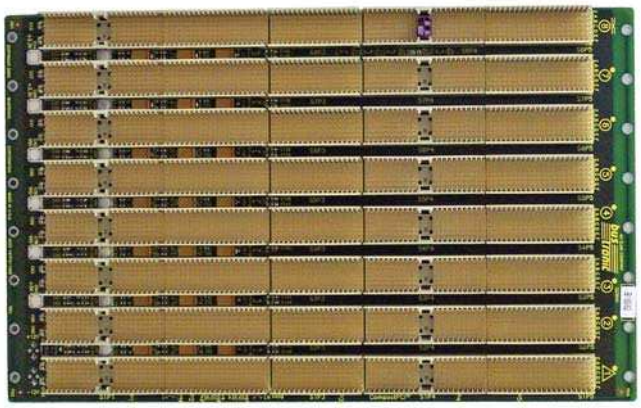
Compact Packet Switching (cPSB) Backplane



Description

The performance of CompactPCI is vastly improved with the cPSB (PICMG 2.16) protocol. It provides the ideal solution for thirdgeneration wireless, Internet protocol, voice over IP (VoIP), and other applications that require high processing power and data rates. CPSB increases system performance by moving data traffic off the shared bus, and onto an embedded switched Ethernet network fabric (10/100/1000 Mbit/s), accessed via the P3 connector.

The 4-slot, 6-slot, and (one of the) 8-slot backplanes have 1 fabric slot, with the rest of the slots as node slots with the CompactPCI bus. Elma Bustronic also offers an 8-slot version with 2 fabric slots, with the rest of the node slots with the CompactPCI bus and with or without the H.110bus. The 16-slot PICMG 2.16 backplane has 2 fabric slots, with the rest of the node slots with the cPCI bus. The cPCI bus segments are bridged (See cPCI Bridge Datasheet). All of Bustronic's standard PICMG 2.16 backplanes offer one slot that is convertible to a system slot via a CPU Enable jumper. With the power studs and power blades dispersed throughout key locations in the backplanes, the overall widths are a true 4-slot, 6-slot, and 8-slot size. (Many CompactPCI backplanes have power bugs on the side ofthe backplane, adding a slot size of width to the dimensions.) This allows the 4-slot, 6-slot, and 8-slot backplanes to fit within 2U, 3U, and 4U horizontal chassis respectively. Further, the use of 6/32 power studs gives the backplanes modularity, allowing power interface boards in various configurations to be mounted to the backplane. Bustronic offers design services for various other configurations of PICMG 2.16. The backplanes have several 6/32 power studs for 3.3V, 5V, V I/O, and GND and fast-on blades for +/- 12V. Per the specification, the shelf geographical addressing is located in the P3 section of the backplane and is configurable. The DEG (derate/degrade) and FAIL headers can be run from the power supply to the CPU board for power supply monitoring. A PRST (power on reset pin) is also included. Some cPSB versions include a 20-pin header with pins for the Intelligent Platform Management Bus (IPMB) for shelf management.

The cPSB backplane is composed of Node Slots , Fabric Slots, and the Links that interconnect them. The cPSB topology is a star topology (not a bus). Each line interconnecting a Node Slot and Fabric Slot represents a Link that is a 10/100/1000 Mbps full-duplex Ethernet connection. Node Boards communicate by transferring/receiving packets to/from the Fabric Board, which transfers the packet to/from one or more Node Boards. Thus, every Node Board can communicate with every other Node Board and form a fabric. A cPSB backplane can have up to twenty Node Slots (with one or two Link Ports) per chassis; and up to two Fabric Slots. The differential pairs are routed as close together as possible and kept on the same layer. The outside layers are ground for EMI protection and suppression. The signal layers are alternated with power or ground layers for controlled impedance and to minimize crosstalk. Power and ground planes are 2 oz. copper. High and low frequency decoupling capacitors are distributed generously across the backplane.

Features

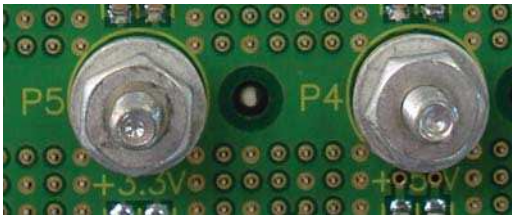
- Conforms to PICMG 2.16 specification
- Conforms to PICMG basic specification 2.0 R3.0
- Moves data via switched Ethernet fabric (10/100/1000 Mbit/s)
- Star and Dual Star topologies
- Versions with and without H.110 telephony bus
- Power studs between slots to save space
- Optional power supply connectors or power bugs
- Supports existing SBCs, Ethernet cards, and line cards
- Controlled impedance stripline design

Board Specifications

- 10-layer board (H.110 14-layer board)
- 2 oz. copper power and ground
- PCB UL recognized 94V-0
- PCB FR-4 or equivalent
- PCB .134" thick (4, 6, & 8 slot w/o H.110), .152" thick (8 & 16 slot w/ H.110)

Mechanical Specifications

- 6U height
- 4, 6, 8, and 16 slot sizes standard
- Ethernet and cPCI compatible



Close-up of 6-32 Power Studs

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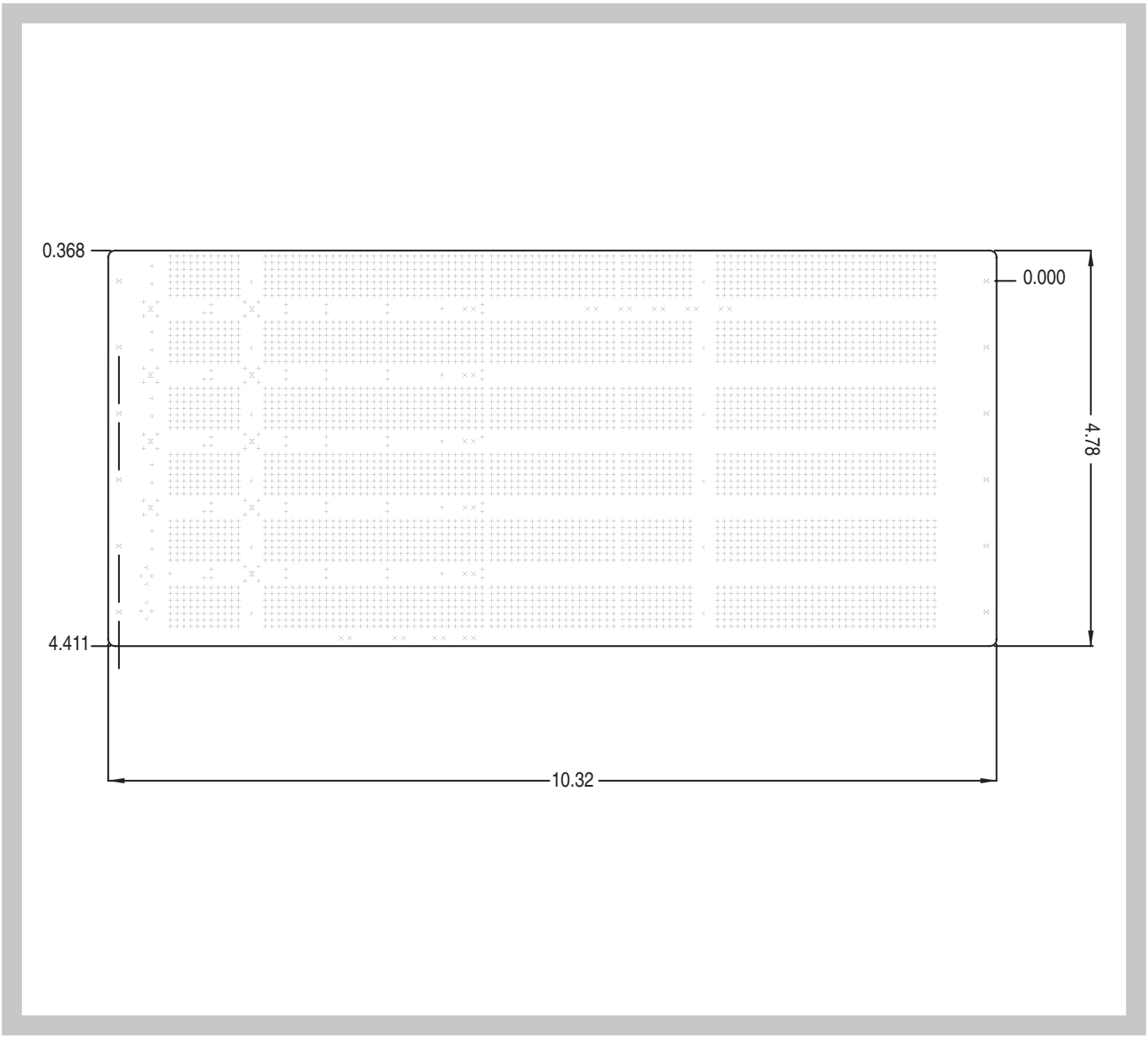
Line Drawing



ORDER INFORMATION

Total Slots	Fabric Slots	Node Slots	Height	Width	Part Number
4	1	2 w/cPCI, 1 node/sys slot w/cPCI	10.32 in.	3.16 in.	107PS11604
4	1	2 w/cPCI and H.110, 1 node/sys slot w/cPCI	10.32 in.	3.16 in.	108PS11604
6	1	4 w/cPCI , 1 node/sys slot w/cPCI	10.32 in.	4.78 in.	107PS11606
6	1	4 w/cPCI and H.110, 1 node/sys slot w/cPCI	10.32 in.	4.78 in.	108PS11606
8	1	6 w/cPCI, 1 node/sys slot w/cPCI	10.32 in.	6.38 in.	107PS11608
8	2	5 w/cPCI, 1 node/sys slot w/ cPCI, IPM Sentry shelf mgmt. connector	10.32 in.	6.38 in.	107PS21608
8	2	5 w/cPCI and H.110, 1 node/sys slot w/cPCI	10.32 in.	6.38 in.	108PS21608
16	2	13 w/cPCI, 1 node/sys slot w/cPCI, bridged	10.32 in.	15.967 in.	107PS22616

Compact Packet Switching (cPSB) Backplane

Product Configurations

(Example: 107PS11608-0157R)

107	Product	Fabric Slots	System Slots	Form	Slots	-_ _ _ _ _Configuration

107 = PICMG 2.16 Compliant
108 = PICMG 2.16 with CTEL, H.110 compatible

Product
PS = Compact Packet Switching Backplane

Fabric Slots
1 = 1 Fabric Slot
2 = 2 Fabric Slots

System Slots
1-9

Form
6 = 6U height

02-21 = Slots

Configuration

Power Interface
0 = 6-32 studs, fast-on blades for +/- 12V

Connectors for P1 & P2
0 = P1 short, P2 long
1 = P1 short, P2 short
2 = P1 short, No P2
X = Not applicable

Connectors for P3, P4 & P5
0 = Not applicable
1 = Not applicable
2 = Not applicable
3 = Not applicable
4 = Not applicable
5 = P3 & P5 long type AB, P4 long type A
X = Not applicable

Shrouds
0 = P2 only
1 = Not applicable
2 = Not applicable
3 = Not applicable
4 = Not applicable
5 = Not applicable
6 = Not applicable
7 = P4 type A , P3 & P5 type AB
X = Not applicable

RoHS
R = RoHS compliant

Common Configurations Examples

-0157 **-0257** **-0157R** **-0257R**

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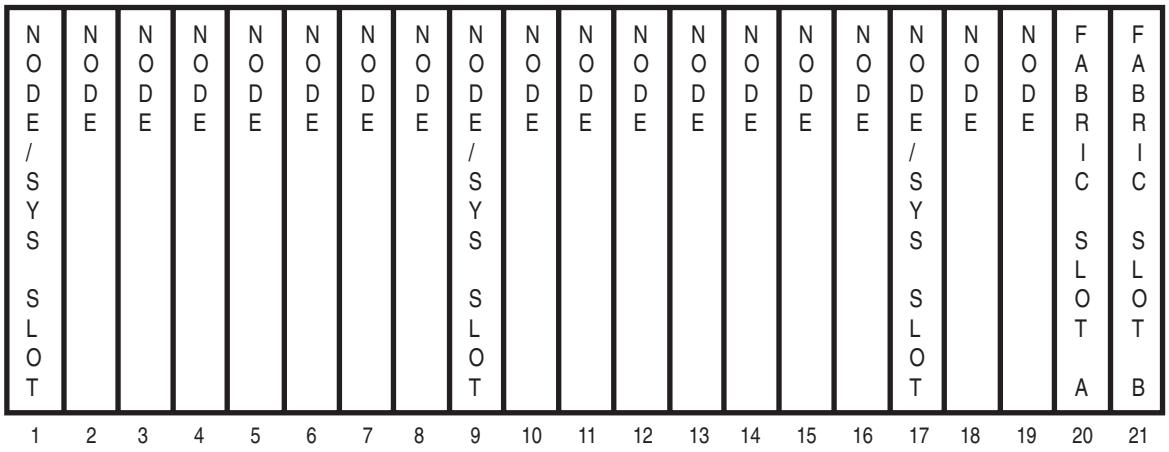
PICMG 2.16 Backplane Standard Configuration



CPSB backplanes can come in various configurations. The CompactPCI and H.110 buses can be implemented or not adopted. One (Star topology) or two (Dual Star) fabric slots can be used. Also, there are various implementations of the system slots, alarm cards, power interfaces, etc. Consult Elma Bustronic for help in developing your configuration.

Pinouts for Compact Switching Backplane

The following pinout tables of the cPSB backplane are for the fabric board slots in P5 and P3, and the node board slots in P3. The P1 and P2 areas of the backplane follow the standard PICMG 2.0 Rev. 3.0 configuration for CompactPCI backplanes and the P4 section follows the Computer Telephony PICMG 2.5 Rev. 1.0 specification. See the CompactPCI Reference Sheet on any CompactPCI page on the Elma Bustronic Web site for other pinouts.

Node Board P3 Pin Assignment

19	GND	BP(I/O) (1,3)	BP(I/O) (1,3)	BP(I/O) (1,3)	BP(I/O) (1,3)	BP(I/O) (1,3)	GND	P3 CONNECTOR
18	GND	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND	
17	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND	
16	GND	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND	
15	GND	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND	
14	GND	BP(I/O) (1,3)	BP(I/O) (1,3)	BP(I/O) (1,3)	BP(I/O) (1,3)	BP(I/O) (1,3)	GND	
13	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
12	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
11	(2)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	(2)	
10	(2)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	(2)	
9	(2)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	(2)	
8	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
7	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
6	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
5	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
4	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
3	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
2	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
1	GND	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	BP(I/O) (1,16)	GND	
Pin	**Z** (5)	**A**	**B**	**C**	**D**	**E**	**F** (6)	

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Fabric Board P5 Pin Assignment

22	GND	LP19_DA+	LP19_DA-	GND	LP19_DC+	LP19_DC-	GND	P5 CONNECTOR
21	GND	LP19_DB+	LP19_DB-	GND	LP19_DD+	LP19_DD-	GND	
20	GND	LP18_DA+	LP18_DA-	GND	LP18_DC+	LP18_DC-	GND	
19	GND	LP18_DB+	LP18_DB-	GND	LP18_DD+	LP18_DD-	GND	
18	GND	LP17_DA+	LP17_DA-	GND	LP17_DC+	LP17_DC-	GND	
17	GND	LP17_DB+	LP17_DB-	GND	LP17_DD+	LP17_DD-	GND	
16	GND	LP16_DA+	LP16_DA-	GND	LP16_DC+	LP16_DC-	GND	
15	GND	LP16_DB+	LP16_DB-	GND	LP16_DD+	LP16_DD-	GND	
14	GND	LP15_DA+	LP15_DA-	GND	LP15_DC+	LP15_DC-	GND	
13	GND	LP15_DB+	LP15_DB-	GND	LP15_DD+	LP15_DD-	GND	
12	GND	LP14_DA+	LP14_DA-	GND	LP14_DC+	LP14_DC-	GND	
11	GND	LP14_DB+	LP14_DB-	GND	LP14_DD+	LP14_DD-	GND	
10	GND	LP13_DA+	LP13_DA-	GND	LP13_DC+	LP13_DC-	GND	
9	GND	LP13_DB+	LP13_DB-	GND	LP13_DD+	LP13_DD-	GND	
8	GND	LP12_DA+	LP12_DA-	GND	LP12_DC+	LP12_DC-	GND	
7	GND	LP12_DB+	LP12_DB-	GND	LP12_DD+	LP12_DD-	GND	
6	GND	LP11_DA+	LP11_DA-	GND	LP11_DC+	LP11_DC-	GND	
5	GND	LP11_DB+	LP11_DB-	GND	LP11_DD+	LP11_DD-	GND	
4	GND	LP10_DA+	LP10_DA-	GND	LP10_DC+	LP10_DC-	GND	
3	GND	LP10_DB+	LP10_DB-	GND	LP10_DD+	LP10_DD-	GND	
2	GND	LP9_DA+	LP9_DA-	GND	LP9_DC+	LP9_DC-	GND	
1	GND	LP9_DB+	LP9_DB-	GND	LP9_DD+	LP9_DD-	GND	
Pin	**Z** [5]	**A**	**B**	**C**	**D**	**E**	**F** [6]	

Fabric Board P3 Pin Assignment

19	GND	SGA4 [4]	SGA3 [4]	SGA2 [4]	SGA1 [4]	SGA0 [4]	GND	P3 CONNECTOR
18	GND	LPf_DA+ [18]	LPf_DA- [18]	GND	LPf_DC+ [18]	LPf_DC+ [18]	GND	
17	GND	LPf_DB+ [18]	LPf_DB- [18]	GND	LPf_DD+ [18]	LPf_DD+ [18]	GND	
16	GND	LP8_DA+	LP8_DA-	GND	LP8_DC+	LP8_DC+	GND	
15	GND	LP8_DB+	LP8_DB-	GND	LP8_DD+	LP8_DD+	GND	
14	GND	LP7_DA+	LP7_DA-	GND	LP7_DC+	LP7_DC+	GND	
13	GND	LP7_DB+	LP7_DB-	GND	LP7_DD+	LP7_DD+	GND	
12	GND	LP6_DA+	LP6_DA-	GND	LP6_DC+	LP6_DC+	GND	
11	(2)	LP6_DB+	LP6_DB-	GND	LP6_DD+	LP6_DD+	(2)	
10	(2)	LP5_DA+	LP5_DA-	GND	LP5_DC+	LP5_DC+	(2)	
9	(2)	LP5_DB+	LP5_DB-	GND	LP5_DD+	LP5_DD+	(2)	
8	GND	LP4_DA+	LP4_DA-	GND	LP4_DC+	LP4_DC+	GND	
7	GND	LP4_DB+	LP4_DB-	GND	LP4_DD+	LP4_DD+	GND	
6	GND	LP3_DA+	LP3_DA-	GND	LP3_DC+	LP3_DC+	GND	
5	GND	LP3_DB+	LP3_DB-	GND	LP3_DD+	LP3_DD+	GND	
4	GND	LP2_DA+	LP2_DA-	GND	LP2_DC+	LP2_DC+	GND	
3	GND	LP2_DB+	LP2_DB-	GND	LP2_DD+	LP2_DD+	GND	
2	GND	LP1_DA+	LP1_DA-	GND	LP1_DC+	LP1_DC+	GND	
1	GND	LP1_DB+	LP1_DB-	GND	LP1_DD+	LP1_DD+	GND	
Pin	**Z** [5]	**A**	**B**	**C**	**D**	**E**	**F** [6]	

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Fabric Board P5 Pin Assignment

22	GND	LP19_DA+	LP19_DA-	GND	LP19_DC+	LP19_DC-	GND	P5 CONNECTOR
21	GND	LP19_DB+	LP19_DB-	GND	LP19_DD+	LP19_DD-	GND	
20	GND	LP18_DA+	LP18_DA-	GND	LP18_DC+	LP18_DC-	GND	
19	GND	LP18_DB+	LP18_DB-	GND	LP18_DD+	LP18_DD-	GND	
18	GND	LP17_DA+	LP17_DA-	GND	LP17_DC+	LP17_DC-	GND	
17	GND	LP17_DB+	LP17_DB-	GND	LP17_DD+	LP17_DD-	GND	
16	GND	LP16_DA+	LP16_DA-	GND	LP16_DC+	LP16_DC-	GND	
15	GND	LP16_DB+	LP16_DB-	GND	LP16_DD+	LP16_DD-	GND	
14	GND	LP15_DA+	LP15_DA-	GND	LP15_DC+	LP15_DC-	GND	
13	GND	LP15_DB+	LP15_DB-	GND	LP15_DD+	LP15_DD-	GND	
12	GND	LP14_DA+	LP14_DA-	GND	LP14_DC+	LP14_DC-	GND	
11	GND	LP14_DB+	LP14_DB-	GND	LP14_DD+	LP14_DD-	GND	
10	GND	LP13_DA+	LP13_DA-	GND	LP13_DC+	LP13_DC-	GND	
9	GND	LP13_DB+	LP13_DB-	GND	LP13_DD+	LP13_DD-	GND	
8	GND	LP12_DA+	LP12_DA-	GND	LP12_DC+	LP12_DC-	GND	
7	GND	LP12_DB+	LP12_DB-	GND	LP12_DD+	LP12_DD-	GND	
6	GND	LP11_DA+	LP11_DA-	GND	LP11_DC+	LP11_DC-	GND	
5	GND	LP11_DB+	LP11_DB-	GND	LP11_DD+	LP11_DD-	GND	
4	GND	LP10_DA+	LP10_DA-	GND	LP10_DC+	LP10_DC-	GND	
3	GND	LP10_DB+	LP10_DB-	GND	LP10_DD+	LP10_DD-	GND	
2	GND	LP9_DA+	LP9_DA-	GND	LP9_DC+	LP9_DC-	GND	
1	GND	LP9_DB+	LP9_DB-	GND	LP9_DD+	LP9_DD-	GND	
Pin	**Z** [5]	**A**	**B**	**C**	**D**	**E**	**F** [6]	

Fabric Board P3 Pin Assignment

19	GND	SGA4 [4]	SGA3 [4]	SGA2 [4]	SGA1 [4]	SGA0 [4]	GND	P3 CONNECTOR
18	GND	LPf_DA+ [18]	LPf_DA- [18]	GND	LPf_DC+ [18]	LPf_DC+ [18]	GND	
17	GND	LPf_DB+ [18]	LPf_DB- [18]	GND	LPf_DD+ [18]	LPf_DD+ [18]	GND	
16	GND	LP8_DA+	LP8_DA-	GND	LP8_DC+	LP8_DC+	GND	
15	GND	LP8_DB+	LP8_DB-	GND	LP8_DD+	LP8_DD+	GND	
14	GND	LP7_DA+	LP7_DA-	GND	LP7_DC+	LP7_DC+	GND	
13	GND	LP7_DB+	LP7_DB-	GND	LP7_DD+	LP7_DD+	GND	
12	GND	LP6_DA+	LP6_DA-	GND	LP6_DC+	LP6_DC+	GND	
11	(2)	LP6_DB+	LP6_DB-	GND	LP6_DD+	LP6_DD+	(2)	
10	(2)	LP5_DA+	LP5_DA-	GND	LP5_DC+	LP5_DC+	(2)	
9	(2)	LP5_DB+	LP5_DB-	GND	LP5_DD+	LP5_DD+	(2)	
8	GND	LP4_DA+	LP4_DA-	GND	LP4_DC+	LP4_DC+	GND	
7	GND	LP4_DB+	LP4_DB-	GND	LP4_DD+	LP4_DD+	GND	
6	GND	LP3_DA+	LP3_DA-	GND	LP3_DC+	LP3_DC+	GND	
5	GND	LP3_DB+	LP3_DB-	GND	LP3_DD+	LP3_DD+	GND	
4	GND	LP2_DA+	LP2_DA-	GND	LP2_DC+	LP2_DC+	GND	
3	GND	LP2_DB+	LP2_DB-	GND	LP2_DD+	LP2_DD+	GND	
2	GND	LP1_DA+	LP1_DA-	GND	LP1_DC+	LP1_DC+	GND	
1	GND	LP1_DB+	LP1_DB-	GND	LP1_DD+	LP1_DD+	GND	
Pin	**Z** [5]	**A**	**B**	**C**	**D**	**E**	**F** [6]	

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