Description
The Elma Bustronic 14-slot Dual Star AdvancedTCA (ATCA) backplanes are compliant to the PICMG 3.0 Rev 3.0 specification. The experts in high-speed differential pair routing, Elma Bustronic’s ATCA backplanes have been simulated and characterized by our signal integrity lab to optimize performance.

Features
• Compliant to PICMG 3.0 Rev 3.0 specification
• Designed to meet 40Gbps (4 x 10G ports) data rates
• Based on design principles of IEEE 802.3ba-2010, 10GBase-KR, and 40GBase-KR4
• Nelco 4000 13-SI high grade laminate material
• Extensive pre-layout and post-layout simulation studies
• Backdrilled to minimize stub reflections
• Very low insertion loss deviation (ILD)
• Dual shelf managers in slot 0, radial IPMB/I2C implementation
• Up to 400W/slot 48VDC distribution to each slot
• 18 layer stripline design
• Test reports available upon request

Board Specifications
• 18-layer board
• 2 oz. copper power and ground
• PCB UL recognized 94V-0
• Nelco 4000 13-SI
• PCB .146” thick

Mechanical Specifications
• 5U height
• 14 slots
• 1.2” pitch

Test set-up of 40G ATCA Backplane
Close-up of AMC connectors used for pluggable shelf managers
ATCA Backplanes - 40G

Performance
The current standards addressing 10GBase-KX4 and 10GBase-KR are:

a) IEEE 802.3-2008 (in the informative Annex 69B of section 5) – released.

b) PICMG 3.1 revision 2 – in process.

Once the limits are defined (and met) for 10Gbps operation over one pair/lane (or a backplane channel), the "40G" operation (over 4 such pairs) can be implied, of course only if crosstalk and skew limits are being met.

Slot Positioning
Dual Star Backplanes and frames require installation of Fabric Boards to provide connectivity between Node Boards. PICMG 3.0 requires Fabric Boards to be installed into the lowest numbered Logical Slots (e.g. Slots 1 & 2). PICMG 3.0 systems may, however, have Fabric Slots/Boards located in any physical slot position. To facilitate system configuration, the Chassis FRU ROM is required to provide a mapping of Logical Slot positions to Physical slot positions.

Through simulation/characterization studies from Bustronic's signal integrity lab, we have found that placing the hub slots in the middle of the backplane generally generates the best results. For more info on Bustronic's simulation studies for ATCA, contact Elma Bustronic.

Update Channel Connections
The update channel connections for the 14-slot Dual Star backplanes are 1-4, 2-3, 5-6, 7-8, 9-10, 11-14, 12-13.

Data Transport

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<tr>
<th>Logical Slot</th>
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</table>

Table 6-12 Base Interface + Fabric Interface Dual Star routing assignments
## ORDER INFORMATION

<table>
<thead>
<tr>
<th>Total Slots</th>
<th>Description</th>
<th>Fabric Slots</th>
<th>Node Slots</th>
<th>Width (in.)</th>
<th>Height (in.)</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>5U Dual Star, 40G</td>
<td>2</td>
<td>12</td>
<td>17.55</td>
<td>9.35</td>
<td>109ATCA514-0003R</td>
</tr>
</tbody>
</table>
Signal integrity simulations performed at Elma-Bustronic have shown that achieving 10Gbps/link performance within the IEEE 802.3-2008 section 5 informative limits is possible with reasonable manufacturing and design practices (i.e., without resorting to expensive materials/processes and without affecting the usual design cycles in a serious manner). Prototype backplanes have been manufactured and tested to the informative limits of IEEE and passed. Testing has been realized with a VNA/PNA and custom fixtures developed in partnership with a well-known high-speed test equipment company.

Channel Design Considerations
Regardless of the path taken to define channel parameters, SI pre-layout analysis is a must in order to guarantee the backplane channels will perform to the desired standard(s). For a large backplane, SI analysis requires significant resources to study all possible “worst case” scenarios: the higher the number of parameters to be met, the larger the number of “dimensions” to be explored in the design space.

When designing a “40G capable” backplane, the layer stack-up and trace geometry have to be chosen as a compromise between multiple factors which influence the channel parameters of interest, factors like:

- The necessary number of routing layers (given by the topology – dual star vs full-mesh vs custom),
- The desired impedance (100-Ohm vs 95-Ohm or 85-Ohm differential impedances),
- The skew (lane-to-lane, if specified, or “within channel”, or intra-pair),
- The skin effect loss (and dielectric loss, as part of insertion loss),
- The need to place ground vias at regular intervals, etc.

In turn, these multiple factors are usually impacted by the manufacturability limits:

- Total backplane thickness & aspect ratio,
- Tight vs loose finished line impedance tolerance,
- Desired glass weave style,
- Copper surface roughness & desired copper foil thickness,
- Antipad geometry,
- Backdrilling requirements (number & depth of levels), etc.
ATCA Backplanes - 40G

14-Slot Dual Star AdvancedTCA Backplane Information

The serial links for Base Interface, Fabric Interface and Update Channel Interface are routed as edge coupled differential strip lines having an impedance of 100 ohms –10%.

- The Telephony Clock Interface is implemented as a MLVDS bussed clock.
- The differential lines for Synchronization Clock Interface are terminated at each end with SMD resistors (case 0603) that are mounted directly to the backplane.

The serial links for Synchronization Clock Interface are routed as edge coupled differential strip lines having an impedance of 130 ohms –10%.

The Hardware Address pins of each physical slot are connected to GND or left open, depending on the logical slot related to each physical slot. In this stage, these connections are made by using a jumper field with 8 positions for each slot. The seven bits that determine the Hardware Address are configured as follows:

<table>
<thead>
<tr>
<th>Logical Slot</th>
<th>Hardware Address (7bit)</th>
<th>Logical Slot</th>
<th>Hardware Address (7bit)</th>
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</thead>
<tbody>
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<td>1</td>
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<td>8</td>
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<tr>
<td>7</td>
<td>47h</td>
<td>14</td>
<td>50h</td>
</tr>
</tbody>
</table>

Power Distribution

The Elma Bustronic ATCA backplane family uses the Positronic VPB series, part number VPB30W8F9300A1. Adequate numbers of 48V 6/32 studs are distributed throughout the backplane.

Materials and Finishes - VPB

- Insulator: Glass-filled polyester, UL 94V-0, blue color.
- Contacts: Precision-machined copper alloy with gold flash over nickel plate.

Electrical Characteristics - VPB

- Contact Current Ratings, per UL 1977
  - Size 16 Power Contacts: 30 amperes continuous, all contacts under load.
  - Size 22 Signal Contacts: 2 amperes nominal rating.
- Initial Contact Resistance;
- Termination to termination:
  - Size 16 Contacts: 0.0022 ohms maximum,
  - Size 22 Contacts: 0.0085 ohms maximum,
- Per IEC 512-2, Test 2b.
- Working Temperature: -55°C to +125°C.
Power Distribution

Common Contact Position Function - VPB
1-16 Low Speed Hardware Management
17-24 High Voltage Metallic Test and Ringing Generator Signals
25 Shelf Ground
26 Logic Ground
27/32 Enables for A and B power
28 A Return
29 B Return
30 A Early
31 B Early
33 A Voltage
34 B Voltage

SIGNAL CONNECTORS
The ZD connector is designed to handle over 5 Gbps speeds over standard FR-4 PCB material. The design includes shielded differential pair signal pins for high-performance.

OTHER CONNECTORS
Shelf Management Connectors
Shmc1 connector goes to the Shmc port on slot 1.
Shmc2 connector goes to the Shmc port on slot 2.

Metal and Ring Connectors
MT1 and MT2 are TYCO 880222-4. It mates to an EI Series receptacle with crimp termination, such as 172142-4 There is also an MT EI Series with IDC termination.

Ring Connector
The Ring connector is a Molex 71231-0005 which mates with the Molex 71694 and 5557 series.

Related Products from Elma Electronic:

- System Platforms – need a chassis for your backplane?
- ATCA Embedded Computing Products – SBCs, Switches, Shelf Managers, and More.

Did you know we also offer with this ATCA backplane?

- ATCA Extenders, AMC load boards, RTMs, test modules
- Thermal or backplane simulation/test, paint/silkscreen, customization, integration