

**TIC-PPC-VPX3a - Freescale 8640D based SBC**  
**Module Profiles: MOD3-PAY-2F2U-16.2.3-2;**  
**MOD3-PAY-2F2T-16.2.5-2; MOD3-PAY-1D-16.2.6-1;**  
**and MOD3-PAY-2F-16.2.7-1**

Elma's Target Application System Guides identify the building blocks necessary to design an Open VPX system targeted for use in compute intensive applications including radar and image processing as well as others requiring high bandwidth signal processing and data distribution. This guide addresses Elma's TIC-PPC-VPX3a 3U single board computer featuring Freescale's MPC8640 processor.

VPX Target Application System Guides take the guess work out of VPX system integration. From initial board selection to final chassis level solution, our Application Guides walk you through the component selection process while ensuring complete interoperability.

**Elma's VPX Target Application System Guides:**

- Identify the optimal starting board and its applicable slot profiles
- Recommend supporting boards based on their profiles and function
- Determine the backplane topology for data flow and application
- Identify a standard OpenVPX backplane profile, or design a backplane profile based on aspects of standard backplane profiles
- Identify standard OpenVPX chassis profile for development or deployment

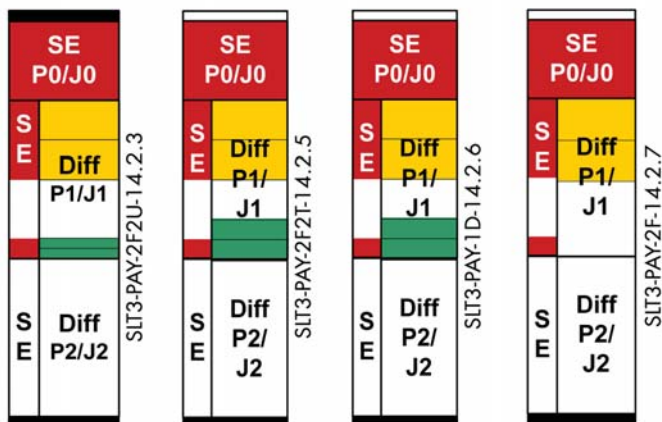
The following Slot Profiles are compliant with the TIC-PPC-VPX3a Single Board Computer:

**Module Profiles:**

- MOD3-PAY-2F2U-16.2.3-2
- MOD3-PAY-2F2T-16.2.5-2
- MOD3-PAY-1D-16.2.6-1
- MOD3-PAY-2F-16.2.7-1

**Slot Profiles:**

- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-2F2T-14.2.5
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7

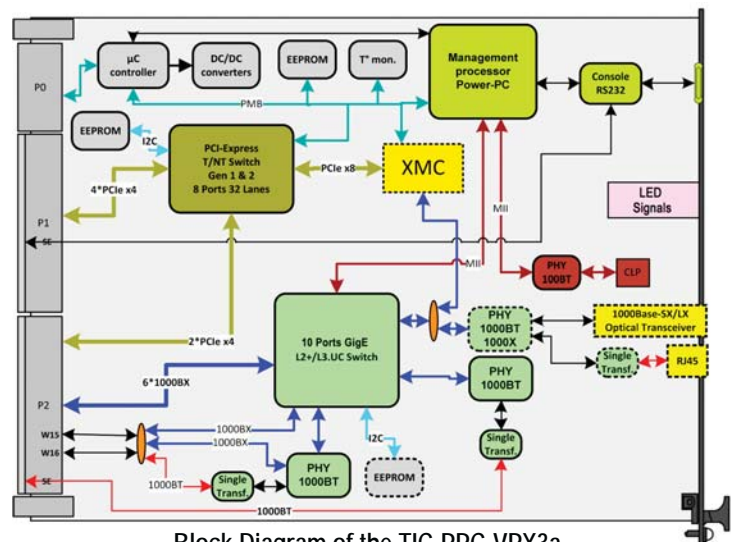


Reference:

- UTP - Ultra Thin Pipe
- TP - Thin Pipe
- FP - Fat Pipe
- DFP - Double Fat Pipe
- QFP - Quad Fat Pipe
- OFF - Octal Fat Pipe



Freescale 8640D Single Board Computer



**Block Diagram of the TIC-PPC-VPX3a**  
*(a full size drawing can be found on the board datasheet)*

**Model Number:** TIC-PPC-VPX3a

**Processor Unit:**

- Single or Dual Core MPC8640(D) 1 GHz Processor

**Communications Interface**

- 2 Gigabit Ethernet ports – 1000Base-T
- Up to 4 rear Ethernet ports – 1000Base-KX
- Optional 2 rear Ethernet ports – 1000Base-T
- Front and rear RS232
- Rear RS422
- 1 PCIe x 4 or SRIO
- 8 PCIe x 1 usable as 2 PCIe x 4 or 4 PCIe x 2

**Optional Rear I/O Transition Module:**

**Model Number:** TIC-PPC-RTM108\_1

- RS232 port (VPX P0 connector)
- RS422 port (VPX P2 connector)
- 8 Single-Ended GPIOs (VPX P2 connector)
- 24 Differential GPIOs (VPX P2 connector) on QSE connector
- Dual 1000Base-BX fiber ports
- Dual 1000Base-T ports copper ports for compatible backplanes



## Companion Boards - OpenVPX Slot Profiles

The supporting boards shown below allow an entire VPX system to be configured and targeted at the needs of compute intensive, high bandwidth signal processing applications. Based on their individual OpenVPX Module Profiles, their function and capabilities, and the application requirements, the following boards are recommended in support of the TIC-PPC-VPX3a Single Board Computer.

Model / Description	Compatible Module Profiles	Compatible Slot Profiles	Slot Profile Samples
 <p><b>T4410a</b> 3U VPX fabric switch with PCIe &amp; GbE ports for data and control plane communication • Six PCIe x4 ports and One PCIe x8 • Eight Gigabit Ethernet ports</p>	MOD3-SWH-6F8U-16.4.10-1,2 MOD3-SWH-6F6U-16.4.1-2,3	SLT3-SWH-6F8U 17*-14.4.9 (per VITA 65 rule 14.4.9.4.1-1) SLT3-SWH-6F6U-14.4.1	
 <p><b>TIC-DC2-VPX3a</b> 3U VPX Intel Core2 Duo SL9380 or SU9300 based Single Board Computer</p>	MOD3-PAY-2F2U-16.2.3-3 MOD3-PAY-2F2T-16.2.5-2 MOD3-PAY-1D-16.2.6-1 MOD3-PAY-2F-16.2.7-1 MOD3-PAY-3F2U-16.2.12-2	SLT3-PAY-2F2U-14.2.3 SLT3-PAY-2F2T-14.2.5 SLT3-PAY-1D-14.2.6 SLT3-PAY-2F-14.2.7 SLT3-PAY-3F2U-14.2.13	
 <p><b>TIC-XMC-VPX3a</b> 3U VPX Carrier Card with one XMC site for multiple configuration options</p>	Multiple, depending on the XMC configuration	Multiple, depending on the XMC configuration	
 <p><b>VPX-5311</b> 3U VPX storage module supports one rotating or solid state SATA drive</p>	MOD3-STO-2U-16.5.1-1,2	SLT3-STO-2U-14.5.1	
 <p><b>TIC-FEP-VPX3b</b> 3U VPX Front End Processor (FEP) board with Xilinx Virtex@-6 FPGA and 1 FMC site • Accepts any VITA 57 FMCs (FPGA Mezzanine Cards)</p>	MOD3-PAY-1F2U-16.2.11-2 MOD3-PAY-1F2F2U-16.2.2-4 MOD3-PER-1F-16.3.2-2	SLT3-PAY-1F2U-14.2.12 SLT3-PAY-1F2F2U-14.2.2 SLT3-PER-1F-14.3.2	

Below are samples of available FPGA Mezzanine Cards (FMCs). Please contact us for more information on the complete range of FMCs available.

200Msps to 2.5Gsps ADC



QUAD 40Msps to 550Msps ADC



QUAD 20Msps to 400Msps ADC



## Identifying a Development Backplane

Many standard OpenVPX backplanes are useful in this next stage of system development. The following standard OpenVPX backplane profiles have been identified as applicable to the architecture described. Seldom will standard profiles meet every requirement; rather they serve as a developmental spring board to the final backplane profile design for the Target Application System.

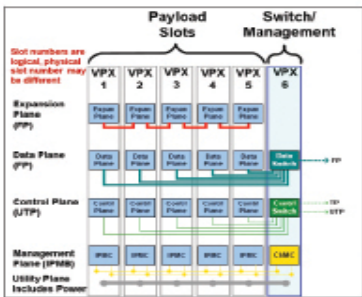
### Available standard VITA 65 OpenVPX Development Backplane Profiles:

BKP3-DIS03-15.2.9-N	Distributed Switch; 1 Payload + 2 Peripheral Slots
BKP3-DIS06-15.2.10-n	Distributed Switch; 1 Payload + 5 Peripheral Slots
BKP3-CEN06-15.2.2-n	Central Switch; 1 Switch + 5 Payload or Peripheral Slots
BKP3-DIS06-15.2.12-n	Hierarchical Switch; 6 Payload or Peripheral Slots

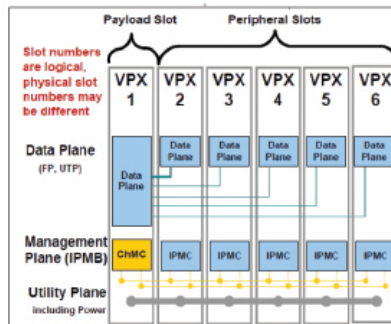


### Topological Diagram of Standard OpenVPX Backplane Profiles:

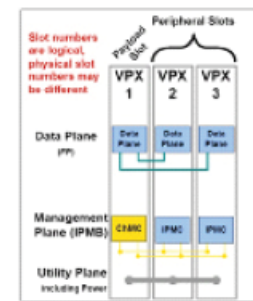
**BKP3-CEN-15.2.2-n**  
1 Switch + 5 Payload or Peripheral



**BKP3-DIS06-15.2.10-n**  
1 Payload + 5 Peripheral



**BKP3-DIS03-15.2.9-n**  
1 Pay + 2 Peripheral Slots

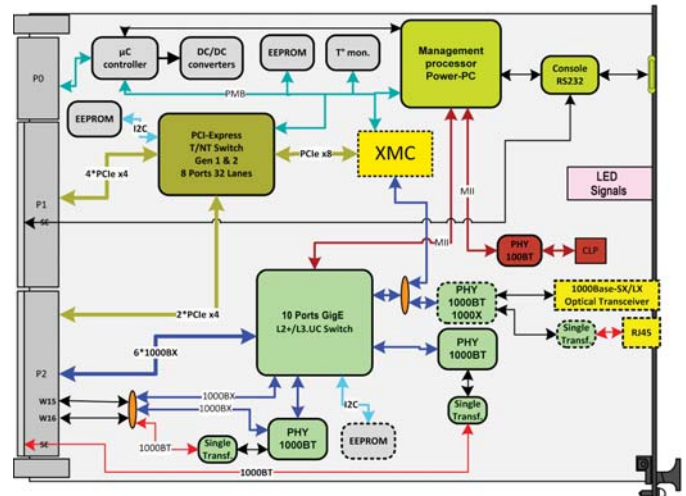
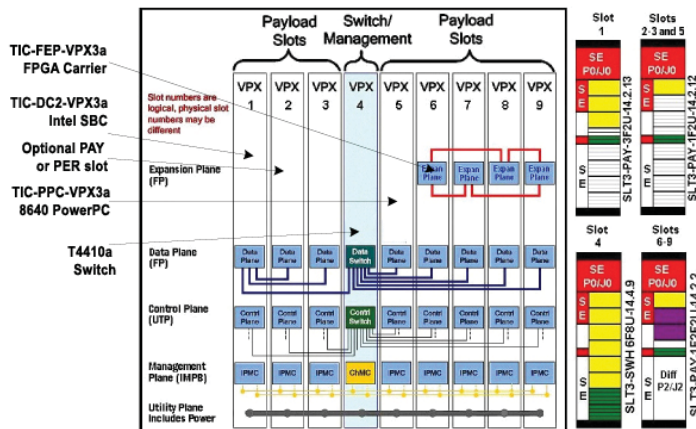


### Topological Diagram of Target Application Backplane Profile BKP3-CEN09-15.2.17-n:

If the end application requires tailoring then a Target Application Profile (TAP) must be developed for the backplane. The backplane shown below is the TAP developed to address the application described. It is based on elements of the standard OpenVPX backplanes listed above and incorporates the slot profiles associated with the identified boards.

Dual cluster, central switched 9-slot backplane with a 4-slot expansion plane mesh for front end computing, and a 6-slot star architecture with 2 leaf nodes for front end computing. Both clusters share the PCIe / Gigabit switch slot.

Block diagram of the T4410 Ethernet/PCIe switch for this TAP System



# OpenVPX Target Application System Guide

Whether it's initial board selection, backplane profile design or integrating the final system, Elma has the knowledge, experience and products to manage VPX system design and provide fully integrated complete chassis level solutions. This system configuration can be adapted for use in various chassis configurations including desktop tower, E-Frame or rack-mount designs.



Description	Environment
<b>E-Frame &amp; Tower Development Platforms</b> - Provides easy access to both sides of the board - Available for 3U and 6U boards - Complete access to rear of the backplane for I/O implementation	Lab, desktop use
<b>19" Rackmount Platforms</b> - 19" rackmount chassis in a wide selection of configurations - Vertical or horizontal board layouts	Standard environmental conditions, such as IT Rooms
<b>Rugged Conduction or Convection Cooled Boxes (ATR)</b> - Available in standard sizes per ATR convection (1/4, 1/2, 3/4, 1) - Accommodates 3U and 6U VPX cards - Supports AC and DC power configurations - Configurable I/O panel for external circular connector	MIL STDs Environments (shock, vibration, heat/cold, etc.); avionics, vetronics, shipboard

## OpenVPX Target Application System Order Information

Your application may require variations from the system described. Consult Elma regarding other configuration options. To get started, order from the following chassis and board options or move to a solution.

### Integrated Chassis Model Number: SEFV3PXCNICXNVN

Description: Nine slot E-frame development chassis with BKP3-CEN09-15.2.17-n backplane, PowerPC SBC hosting Virtex FPGA, T4410 Ethernet/PCIe Switch, TIC-FEP-VPX3b including Virtex-6 with SX315T FPGA and TIC-DC2-VPX3a SBC. Includes Linux 2.6.35 Kernel CentOS chassis software development kit.

### Chassis Model Number: 39E09BWX98Y2VCHX

84HP wide E-Frame development chassis with a 9-slot, 3U OpenVPX backplane designed to Profile BKP3-CEN09-15.2.17-n

### Convection Cooled SBC Model Number: TIC-PPC-VPX3a 882-0x0-740

### Conduction Cooled SBC Model Number: TIC-PPC-VPX3a 882-0x0-795

### Engineering Kit Order Number: 882-001-ENG

### Software Development Kit Order Number: TICLinux\_SDK

