An Elma Bustronic White Paper

OpenVPX Backplane Profiles: Making Sense of System Interoperability For VPX

Introduction

OpenVPX has opened up new definitions for VPX backplanes and systems. This includes defined Module Profiles, Slot Profiles, backplane & chassis configurations, secondary expansion fabrics and control planes, and higher speed fabric options. Elma Bustronic will provide some clarity for the new definitions and what they entail. We'll provide an overview of the various elements involved, and include a couple of potential backplane configurations. The paper will include diagrams on module and slot profile examples, illustrate signal changes for existing VPX products, and configuration examples.

Elma Bustronic

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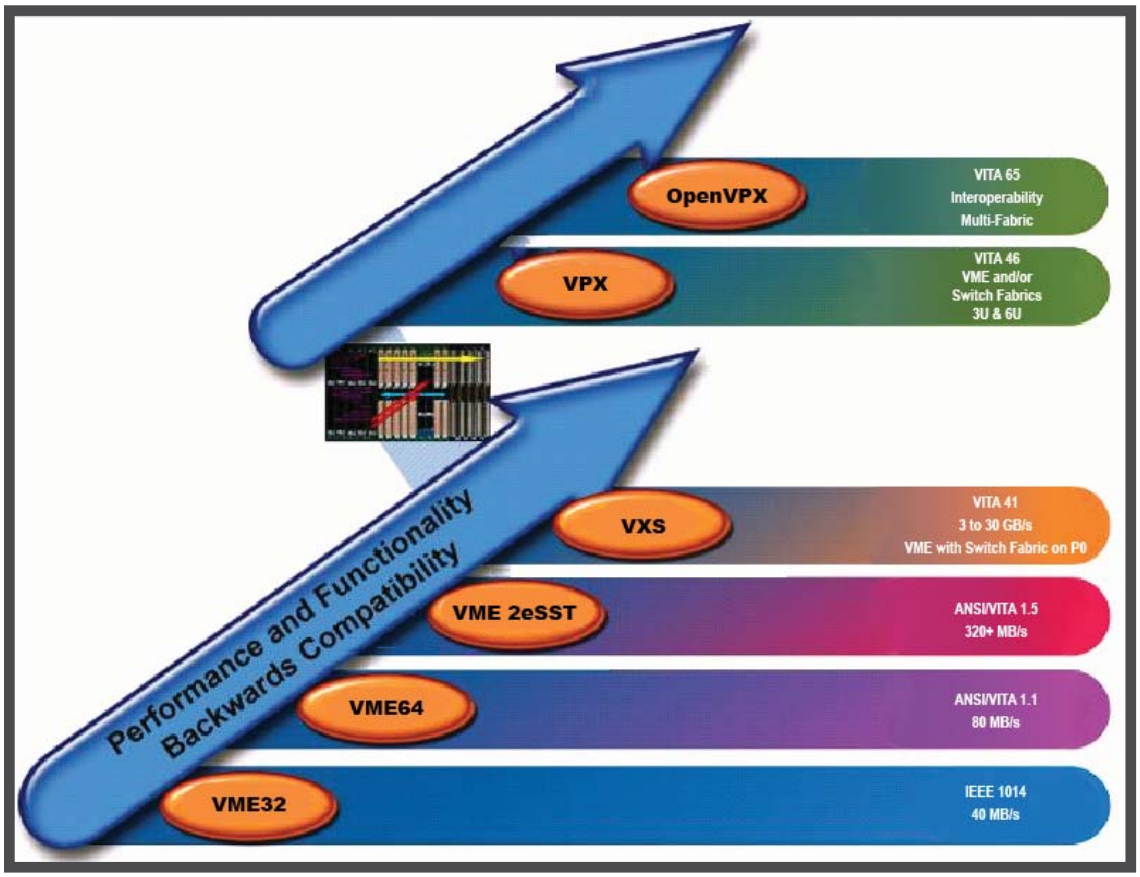
Background of VPX

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is a proposed ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

Technologies called for in VPX include:

- Both 3U and 6U formats
- New 7-row high speed connector rated up to 6.25 Gbps
- Choice of high speed serial fabrics
- PMC and XMC (VITA 42) mezzanines
- Hybrid backplanes to accommodate VME64, VXS and VPX boards



Overview of OpenVPX and VITA 65

OpenVPX is a process that defines system level VPX interoperability for multi-vendor, multi-module, integrated systems environment. The OpenVPX process defines clear interoperability points necessary for integration between Module to Module, Module to Backplane and Chassis. The OpenVPX V1.0 Specification, developed by VITA members, has been turned over to the VSO in October 2009 as VITA 65 for final comment, ballot, and ratification as a standard.

The OpenVPX charter is to:

- Control and manage the assignment of VPX pins to functional planes in an interoperable architecture
- To get a high-degree of interoperability, while leaving room for sensor- / application-specific augmentation
- To make the process of developing VPX-based solutions from the lab to the field much more efficient in cost, time, quality, and repeatability

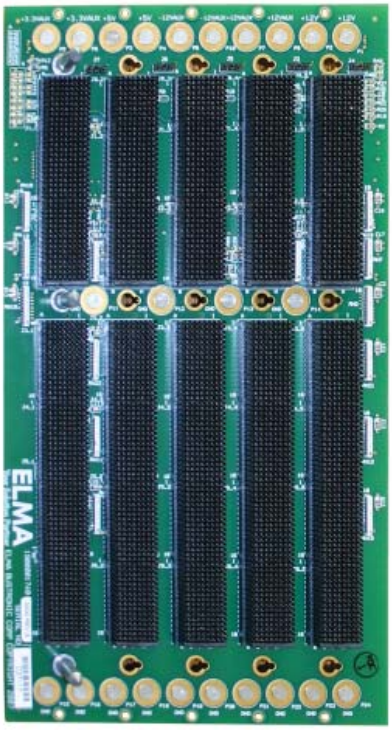
Leverage VITA

- Build upon the efforts of the VITA dot specifications
- Ensure critical functions interoperate through the development of an architecture
- Follow baseline VITA Policy and Procedures
- Submit the final work product through VITA 65 for consideration and adoption

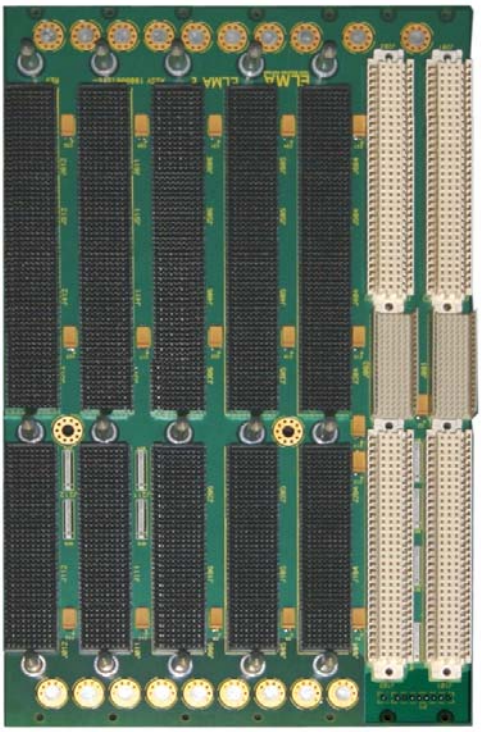
The result of the efforts was that OpenVPX provided a descriptive language for identifying module requirements and backplanes capability. It also provided with the part number configuration more information on the control and fabric planes, including the signal speeds.

Existing Backplanes - Pinout changes

Not all VPX backplanes need to be or will be compliant to VITA 65 (OpenVPX). Only a portion of the applications will require the changes. If you have an existing VPX backplane from before Oct 2009, it is still fully VITA 46.0 compliant. However, it will not be VITA 65 compliant. Unless specified by the customer, Bustronic will design the majority of its VPX backplanes to be in compliance to the subspecification.



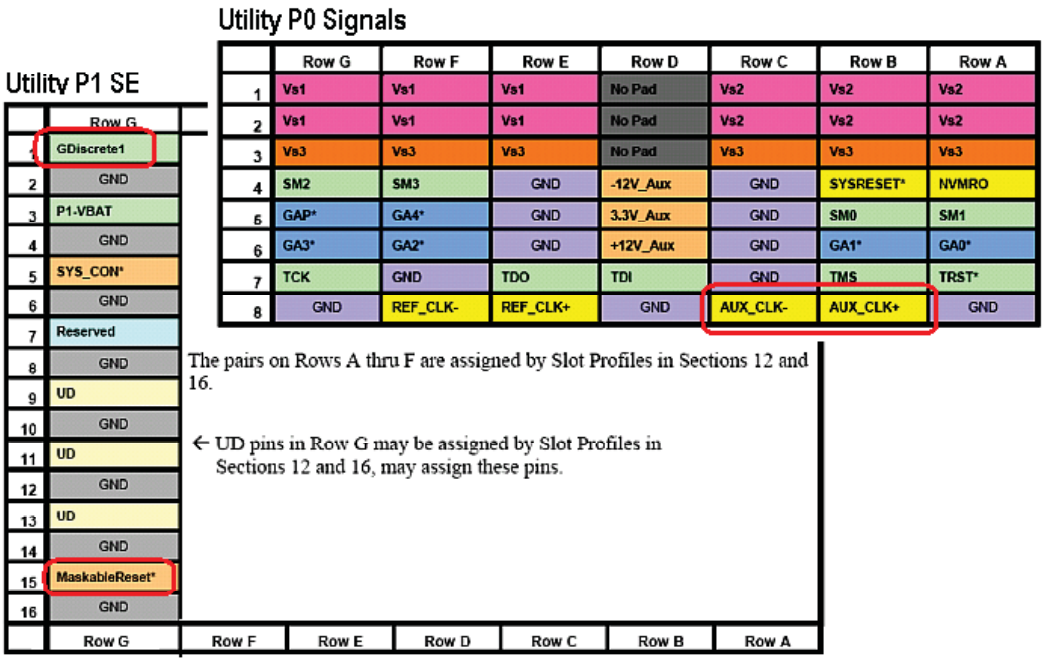
5-slot, 6U VPX Backplane



7-slot VPX Hybrid Backplane

Existing Backplanes - Pinout changes

OpenVPX redefined two reserved P0/J0 signals Aux_Clk (+/-) and added one P1/J1 single ended Utility signal of Maskable Reset and redefined the Res_Bus signal to GDiscrete. The Aux_Clk and GDiscrete pins were already bussed anyway, so there is minimal effect. The SysCon signal is also now configurable.



Backplane and Daughter Card Pinout Chart

Plug in Module P2-P6			Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2-J6			Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	X16 using [15:0]	x8 using [7:0] x4 using [3:0]	SEwafer1	GND	GND-J2	LN0-TD-	LN0-TD+	GND	GND-J2	LN0-RD-	LN0-RD+
2			GND	LN1-TD-	LN1-TD+	GND-J2	GND	LN1-RD-	LN1-RD+	GND-J2	GND
3			SEwafer3	GND	GND-J2	LN2-TD-	LN2-TD+	GND	GND-J2	LN2-RD-	LN2-RD+
4			GND	LN3-TD-	LN3-TD+	GND-J2	GND	LN3-RD-	LN3-RD+	GND-J2	GND
5		x8 using [7:0] x4 using [7:4]	SEwafer5	GND	GND-J2	LN4-TD-	LN4-TD+	GND	GND-J2	LN4-RD-	LN4-RD+
6			GND	LN5-TD-	LN5-TD+	GND-J2	GND	LN5-RD-	LN5-RD+	GND-J2	GND
7			SEwafer7	GND	GND-J2	LN6-TD-	LN6-TD+	GND	GND-J2	LN6-RD-	LN6-RD+
8			GND	LN7-TD-	LN7-TD+	GND-J2	GND	LN7-RD-	LN7-RD+	GND-J2	GND
9		x8 using[15:8] x4 using [11:8]	SEwafer9	GND	GND-J2	LN8-TD-	LN8-TD+	GND	GND-J2	LN8-RD-	LN8-RD+
10			GND	LN9-TD-	LN9-TD+	GND-J2	GND	LN9-RD-	LN9-RD+	GND-J2	GND
11			SEwafer11	GND	GND-J2	LN10-TD-	LN10-TD+	GND	GND-J2	LN10-RD-	LN10-RD+
12			GND	LN11-TD-	LN11-TD+	GND-J2	GND	LN11-RD-	LN11-RD+	GND-J2	GND
13		x4 using[15:12]	SEwafer13	GND	GND-J2	LN12-TD-	LN12-TD+	GND	GND-J2	LN12-RD-	LN12-RD+
14			GND	LN13-TD-	LN13-TD+	GND-J2	GND	LN13-RD-	LN13-RD+	GND-J2	GND
15			SEwafer15	GND	GND-J2	LN14-TD-	LN14-TD+	GND	GND-J2	LN14-RD-	LN14-RD+
16			GND	LN15-TD-	LN15-TD+	GND-J2	GND	LN15-RD-	LN15-RD+	GND-J2	GND

This chart shows the specification pinout of both the Backplane and daughtercard for J2-J6. Note the differences between the plug-in module and the backplane (even and odd pins) for Row E and Row B. Although the number of rows is different, the connector arrangement allows single-ended signals in these areas. The backplane and daugthercard connectors mate without issue.

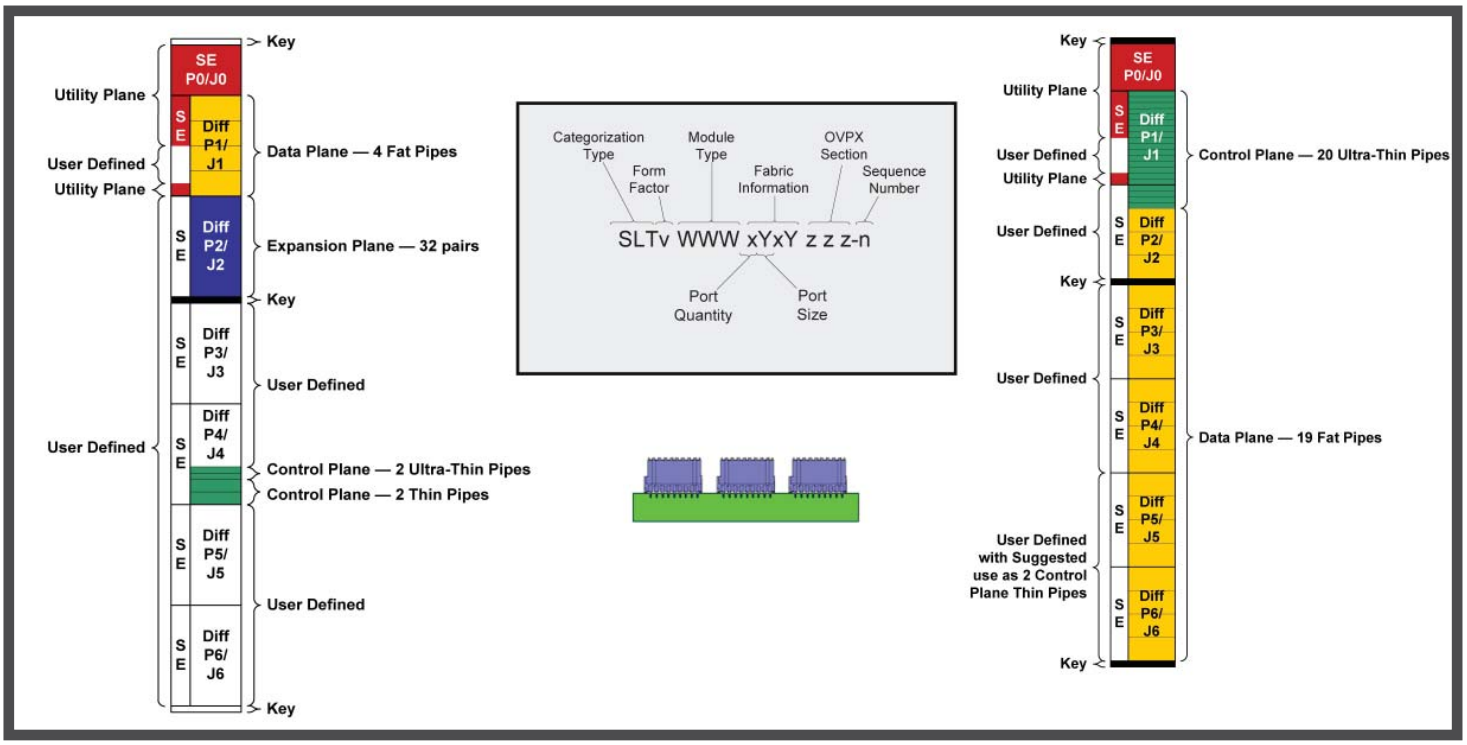
Types of Profiles

There are 3 types of Profiles/Configurations defined: Slot and Module Profiles, and Backplane Configurations. Each VPX module will have a specific chart of backplane signal assignments which will be registered and will define a Module Profile. Backplanes will have Slot Profiles designed to support specific VPX modules. A backplane Slot Profile may accept more than one type of Module Profile. Backplanes will be described as collections of various Slot Profiles. Backplane configurations will be further defined by how the various fabrics or planes within each Slot Profile are interconnected from slot to slot. OpenVPX modules or blades will include “peripheral” cards or “switch” cards.

BP Height	Number of Profiles Defined*	Number of BP Configurations Defined*
3U	22	11
6U	13	13

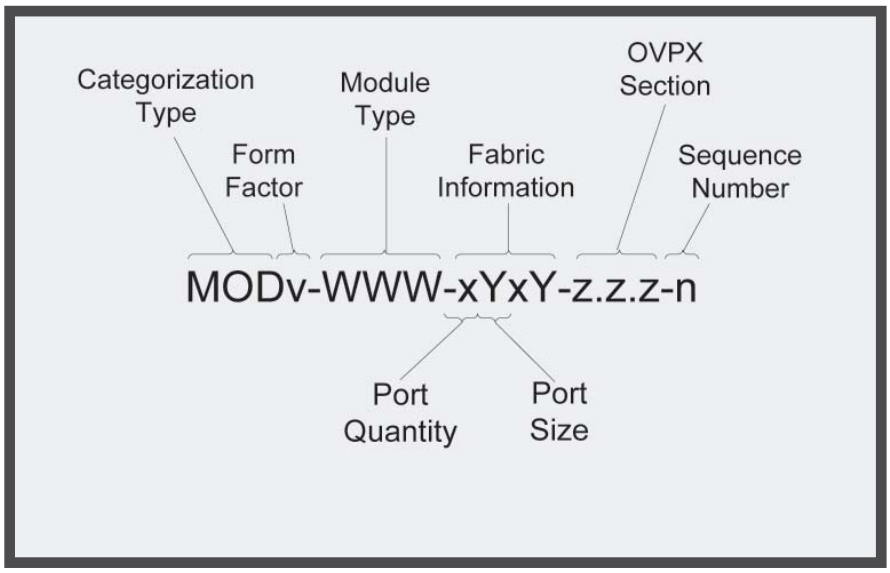
**as of Nov 1, 2009*

OpenVPX Module and Slot Profile Examples



OpenVPX Module and Slot Profile Examples

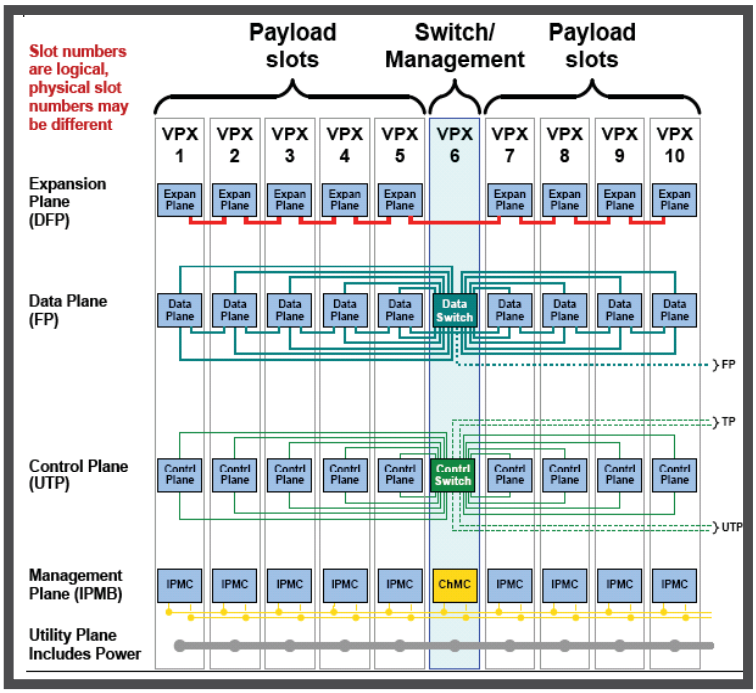
Profile name	Mechanical		Slot Profiles and Section		Channel Gbaud Rate	
	Pitch (in)	RTM Conn	Payload	Switch	Control Plane	Data Plane
BKP3-DIS06-15.2.6-1	1.0	VITA 46.10	SLT3-PAY-2F2T-14.2.5	SLT3-SWH-2F24U-14.4.3 or SLT3-SWH-2F8U-14.4.5	1.25	3.125

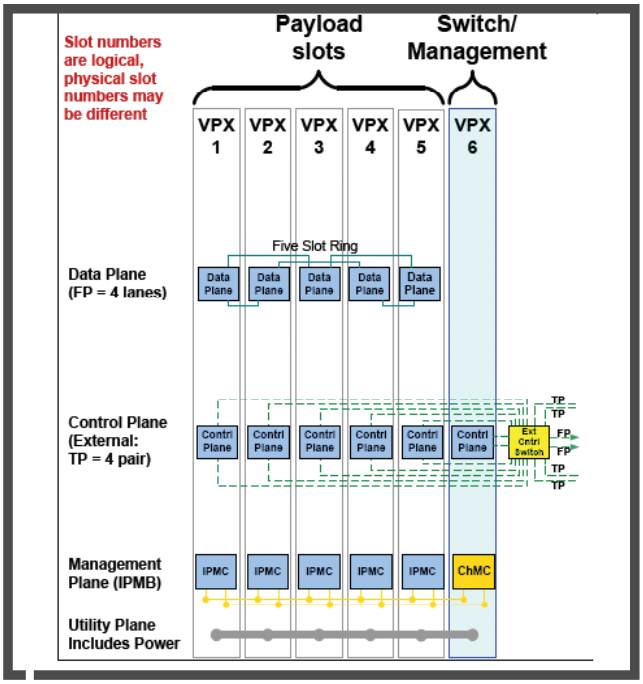


Profile name	Data Plane 4 FP				Control Plane 2 TPs	
	DP01	DP02	DP03	DP04	CPtp01	CPtp02
MOD6-PAY-4F2T-12.2.2-1	SRIO 1.3 at 3.125 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	

The VPX Modules and Slots across the backplanes have been given definitions so that similar Modules will work within certain Slot configurations. The module profile table describes the card height (3U or 6U), type of switch (Payload, Switch, or Bridge), and the fabric and data rates across the data and control planes. The backplane slot profile table describes the height, type of slot (centralized, distributed or hybrid), the pitch, RTM connector, the corresponding payload and switch cards that plug in, and the control and dataplane data rates.

OpenVPX Backplane Configuration Examples

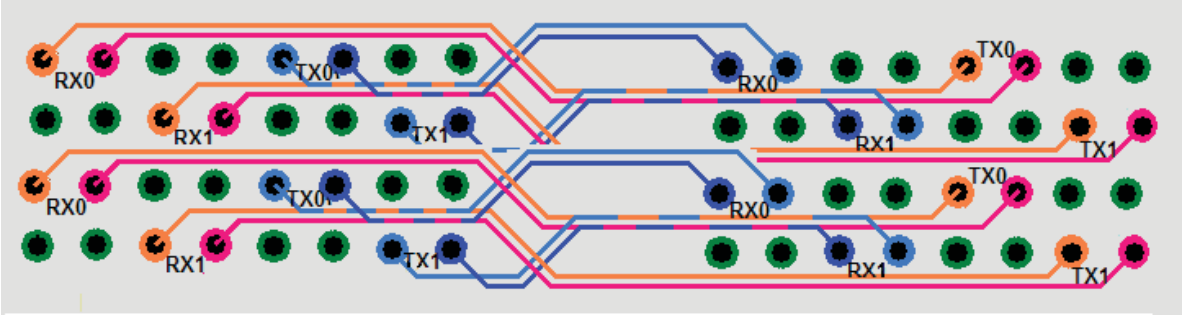




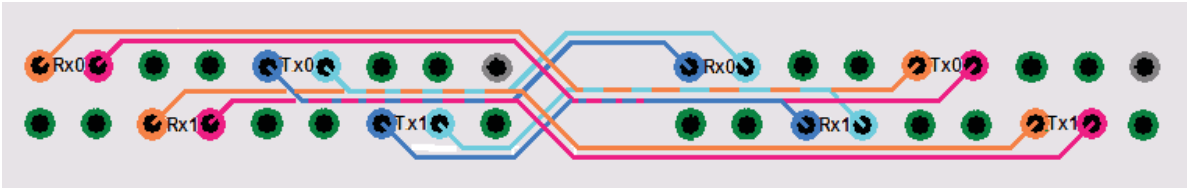
The backplane configuration examples show the connectivity across the backplane for various planes. This includes the routing topology across the data plane and the connections across the expansion, control, management and utility planes. They also provide an illustration of the slot types, whether payload, switch or legacy bus slots.

Types of Channel Signals

Fat Pipe: A channel that is comprised of four links (4 Tx pairs + 4 Rx pairs) is now being referred to as a fat pipe or by use of the x4 nomenclature. 10Gbps capable 10GBase-KX4, 10GBase-BX4, 10GBase-T, PCIe-x4, sRIO-x4, Infiniband-x4



Thin Pipe: A channel that is comprised of two links (2 Tx pairs + 2 Rx pairs) is now being referred to as a thin pipe or by use of the x2 nomenclature. 5Gbps capable 10/100/1000Base-T, 1000Base-BX, PCIe-x2, sRIO-x2, Infiniband-x2



Ultra-thin Pipe: A channel that is comprised of one link (1 Tx pair + 1 Rx pair) is now being referred to as an ultra-thin pipe or by use of the x1 nomenclature. 10GBase-KR, IGBase-KX, PCIe-x1, sRIO-x1, Infiniband-x1a

Summary

OpenVPX provides an easier way to ensure interoperability between OpenVPX systems. The VPX Modules and Slots across the backplanes have been given definitions so that similar Modules will work within certain Slot configurations. The backplane Configurations have been defined to show the collection of Slot profiles it entails, including information on the data rate, routing topology, and fabric used. Now, the integrator can determine that a daughter card Module from “X” company can be used in the same backplane slot as “Y” company’s, when both Module Profiles specify the same Slot Profile.

Ancillary Efforts

There are new efforts that are underway as a result of OpenVPX steps. This include an RF connector interface, an optical connector interface, and a definition of data rates across VPX.

VITA 66 – (formerly 46.12) Optical Connector Interface.
VITA 67 – (formerly 46.14) Mixed Signal RF Connector Interface
VITA 68 – Channel Definition

Elma Bustronic Corporation
Phone: 510.490.7388
Email: sales@elmabustronic.com
www.elmabustronic.com