

JEFF'S PICKS: C4ISR/EW Modular Open Standards Supported on 3U VPX Backplane

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Many military systems depend heavily on open standard slot-card style embedded computing technologies such as VME, CompactPCI, MicroTCA and OpenVPX. And a key piece of those system architectures are the backplanes such boards plug into. As processor and serial interconnect speeds have ramped up over the years, backplane designs have had to keep pace with designs that can handle higher speeds but also all the tricky effects that come into play at GHz level speeds and beyond.

Adding more twists to backplane complexity, new standards and technologies emerged to accommodate coaxial/RF interconnects implemented directly on backplanes and slot cards. And support for ever faster revs of Ethernet, PCI Express, Serial RapidIO brought along new challenges as well. OpenVPX in particular ushered in new varieties of backplanes supporting lengths between one and twenty-one slots. Meanwhile, there are many different profiles available for OpenVPX backplanes—such as central switch topologies, and distributed topologies and root-leaf topologies.

This month's Jeff's Pick section looks at backplane solutions. COTS Journal evaluated several such products on three aspects: technology leadership. The winning product is Elma Electronic's high speed 3U VPX backplane that supports multiple functions including mixed payload modules, single board computers, switches and RF payloads for use by the DoD's Hardware/Software Convergence Initiative (Figure 1). A unique aspect to this backplane is its support of high speed signals on all the data paths as well as leading edge VITA 67.3 connectors compatible with legacy VITA 67.1 and VITA 66.4 RF and optical I/O connectors. According to Elma, this was also the first VPX backplane with a radial slot card for timing and synchronization



Figure 1. Jeff's Pick is Elma Electronic's high speed 3U VPX backplane. It supports multiple functions including mixed payload modules, single board computers, switches and RF payloads for use by the DoD's Hardware/Software Convergence Initiative.

The 3U, 12-slot backplane includes 7 slots that receive radial clock signals (Aux Clk and Ref Clk) driven independently from a radial clock timing card. The remaining 5 slots receive standard VPX bussed Aux_Clk and Ref_Clk signals. The timing card slot also supports a VITA 67.3c connector with 10 SMPM cavities. The backplane can handle the highest data rates possible with the VPX connector through its multiple data plane UTP connections at 10GBASE-KR data rates and 10GBase-KR UTP control plane connections. Four payload slots, each equipped with a combination VITA 67.3c optical and RF connector in the J2 position are also featured on the backplane. The slot 2 switch supports a VITA 67.3d connector module compatible with a payload module fitted with a VITA 66.4 MT optical ribbon connector or a VITA 67.1 RF coaxial connector.

When equipped with optical interfaces, the VPX architecture now allows data rates across the backplane far greater than any copper interconnect can be expected to achieve with the additional benefit of lower design complexity. The VPX optical interface ensures that this backplane will be able to meet all future bandwidth requirements. Also included on the backplane is a 12-cavity, VITA 67.3e connector to support an RF switch card. The new VITA 67.3 connectors allow high speed optical and RF interfaces present on payload modules to be mated and removed from the backplane. The scheme allows different types of I/O cabling routed to a slot to remain connected to the rear of the backplane to distribute interfaces. The backplane is designed to align with the DOD's Hardware/Software Convergence Initiative, which aims to develop a common, modular hardware architecture across C4ISR and EW systems.

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